

IC (Top View)

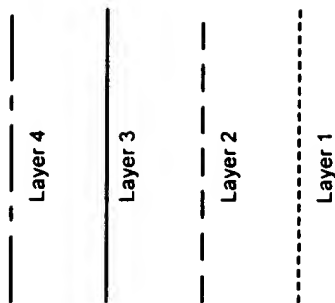
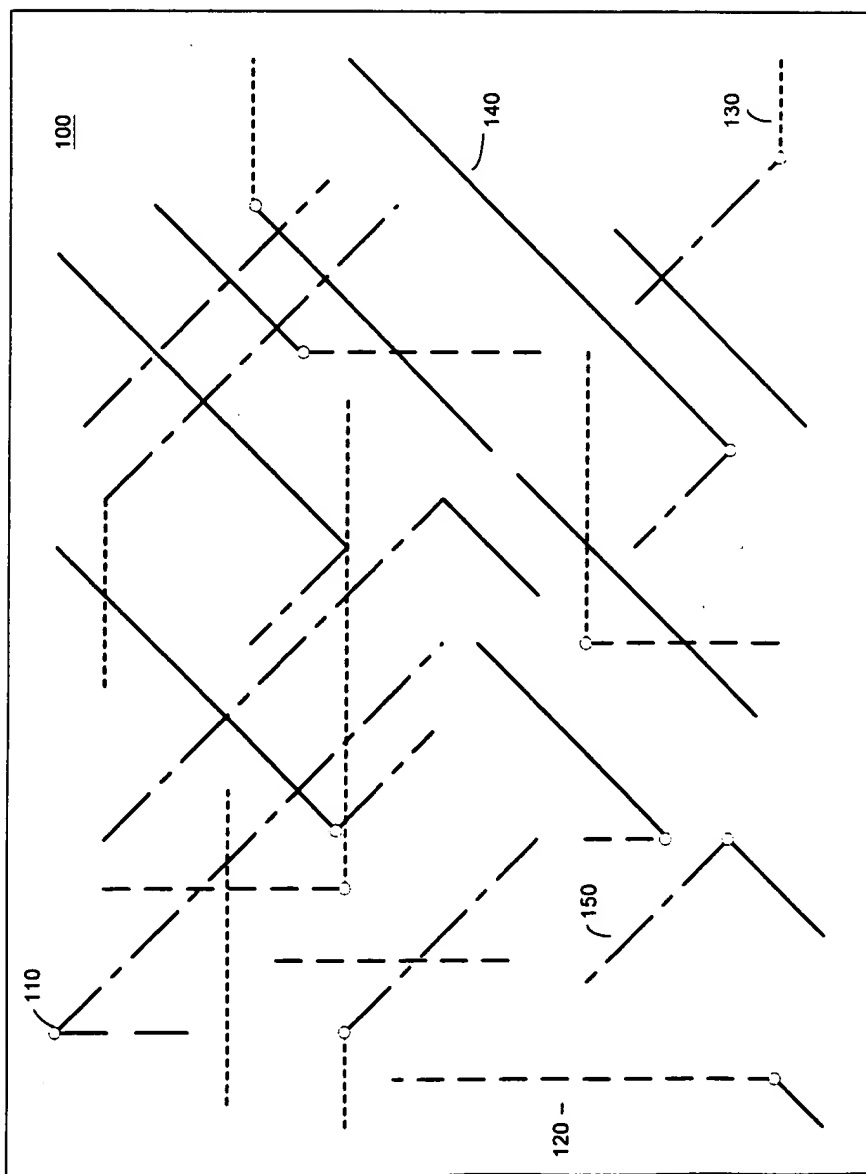


Figure 1a

IC (Top View)

155

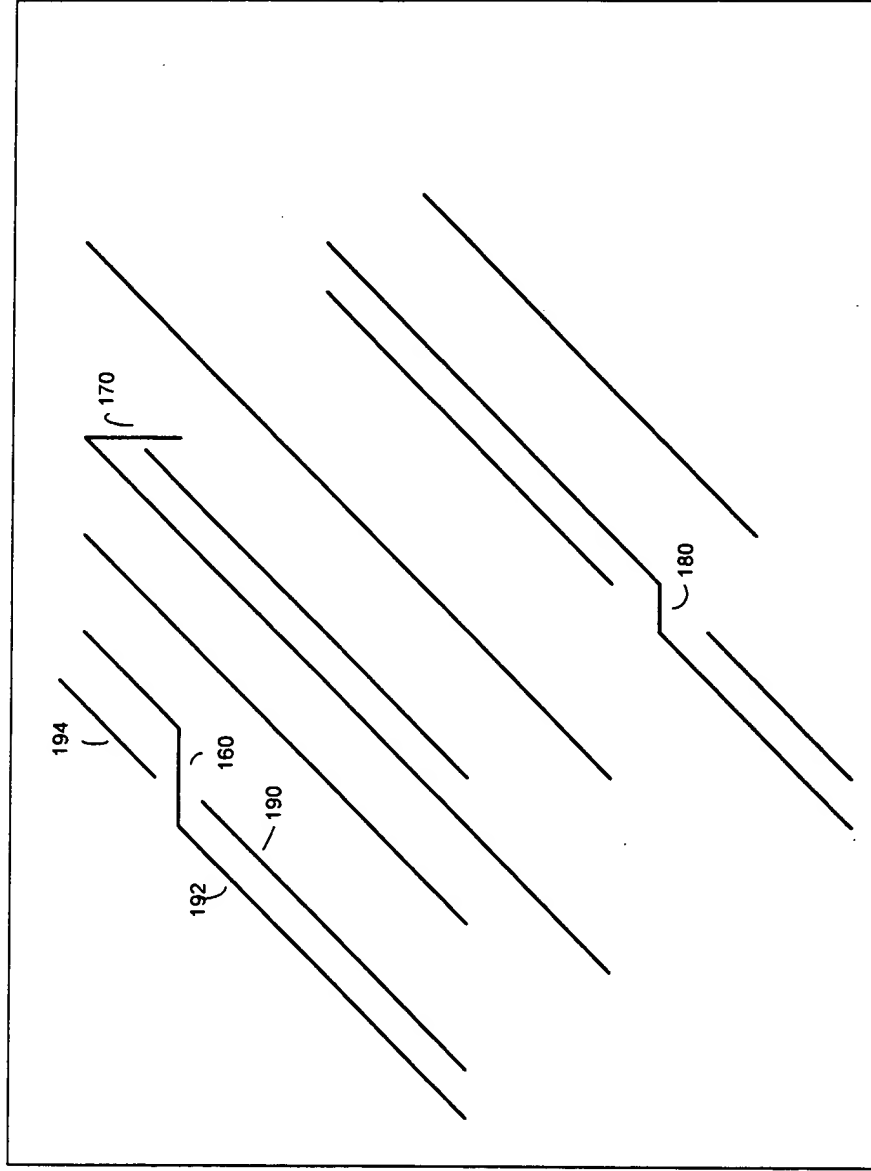
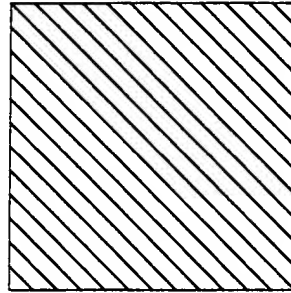
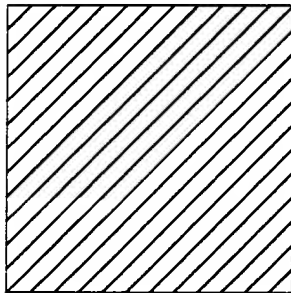


Figure 1b



Layer "n+1"

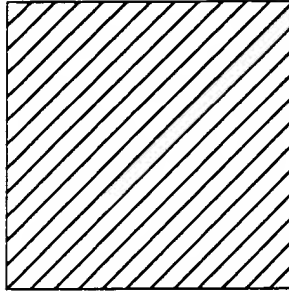
Octalinear (-45 Deg.)



Layer "n"

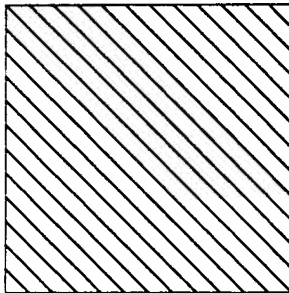
Octalinear (+45 Deg.)

Figure 2a



Layer "n+1"

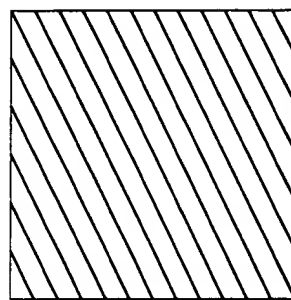
Octalinear (+45 Deg.)



Layer n

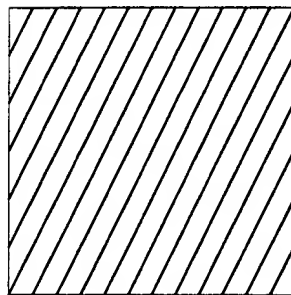
Octalinear (-45 Deg.)

Figure 2b



Layer "n+1"

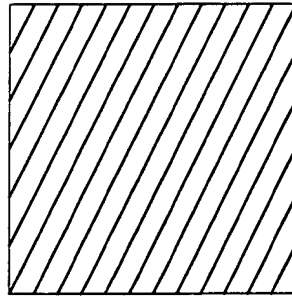
(-60 Degrees)



Layer "n"

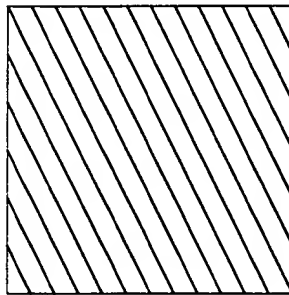
(+60 Degrees)

Figure 3a



Layer "n+1"

(+60 Degrees)



Layer "n"

(-60 Degrees)

Figure 3b

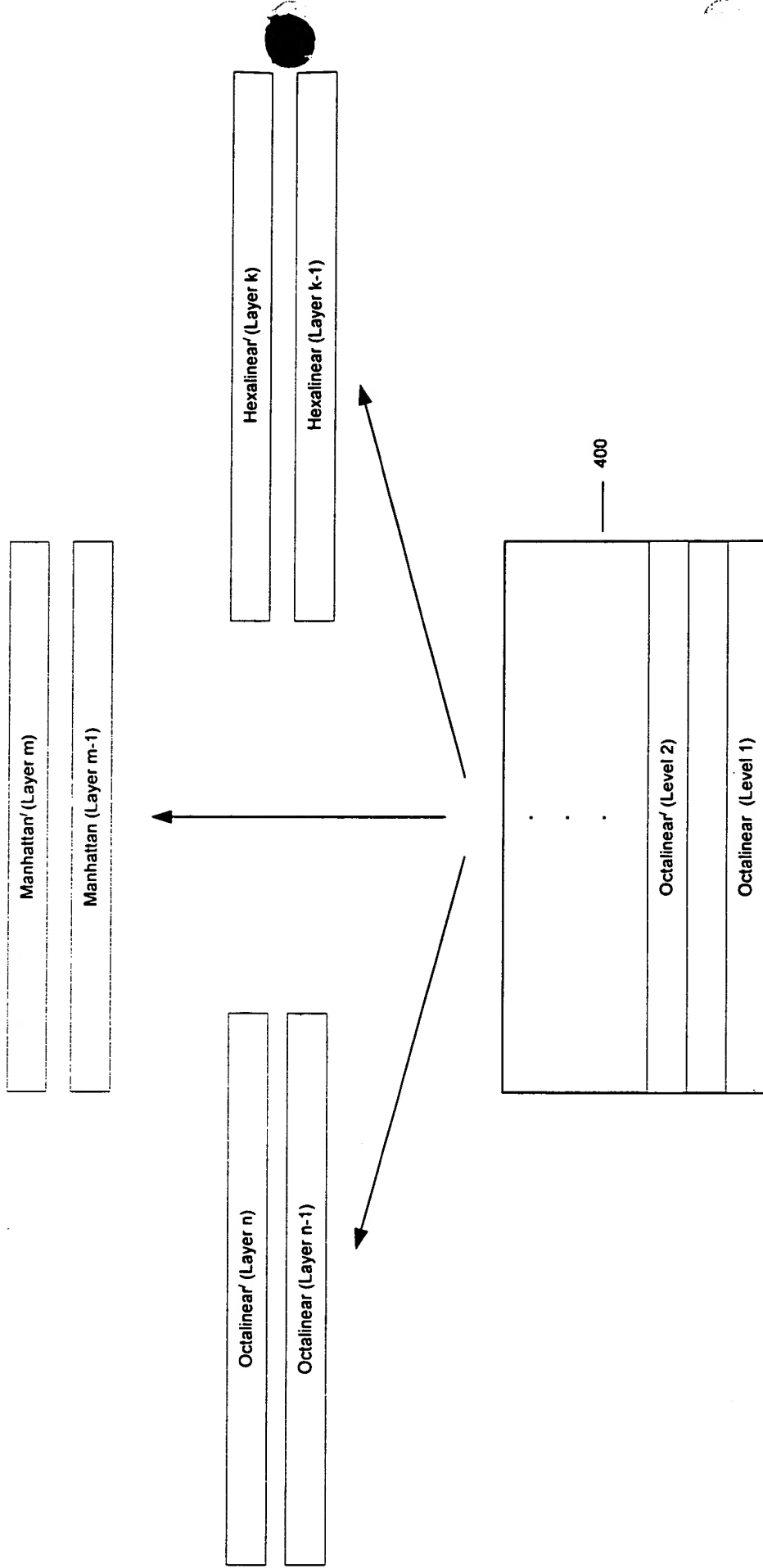


Figure 4a

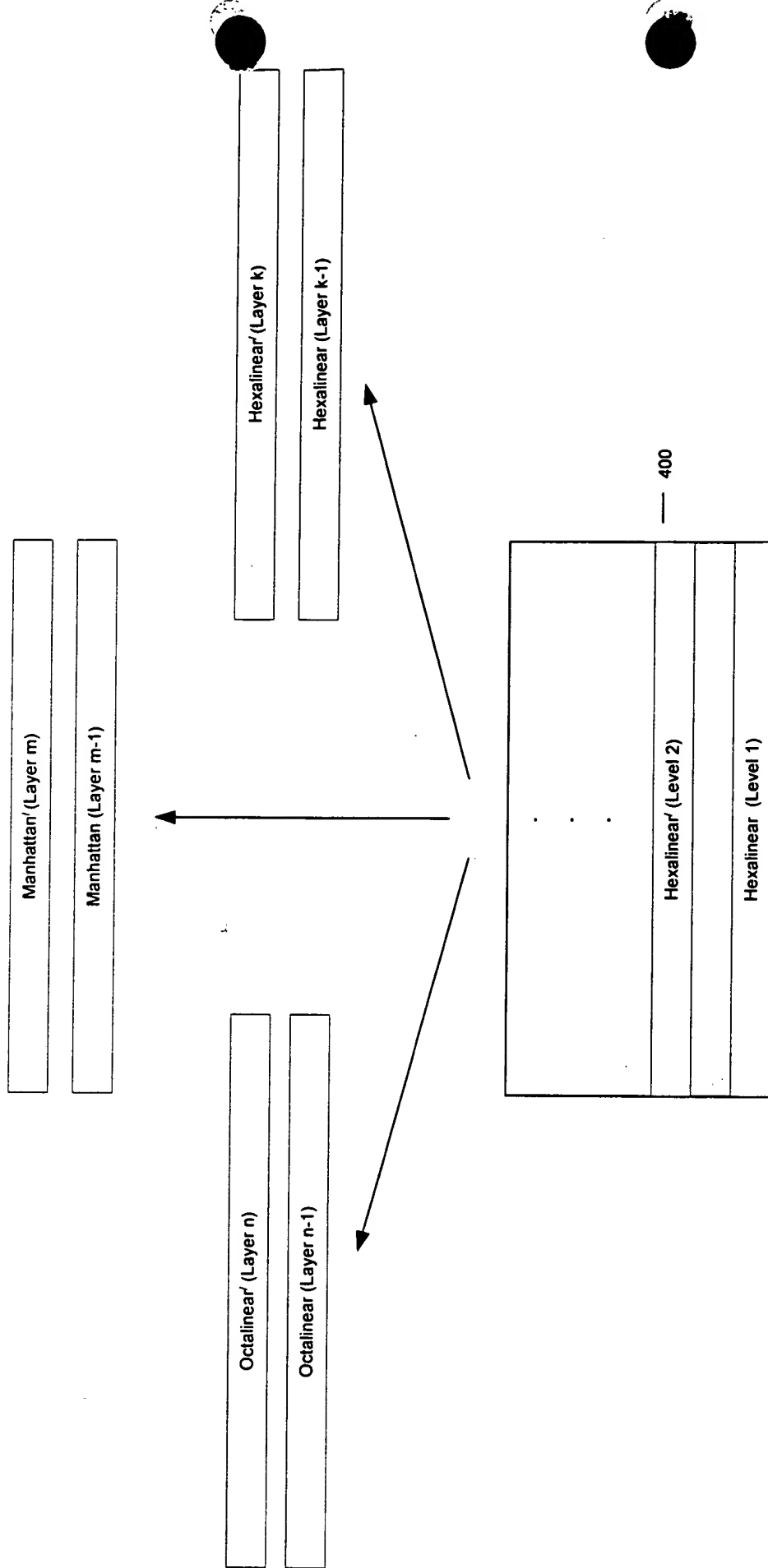


Figure 4b

500

Octalinear Layer 5
Octalinear Layer 4
Manhattan Layer 3
Manhattan Layer 2
Manhattan Layer 1

Figure 5a

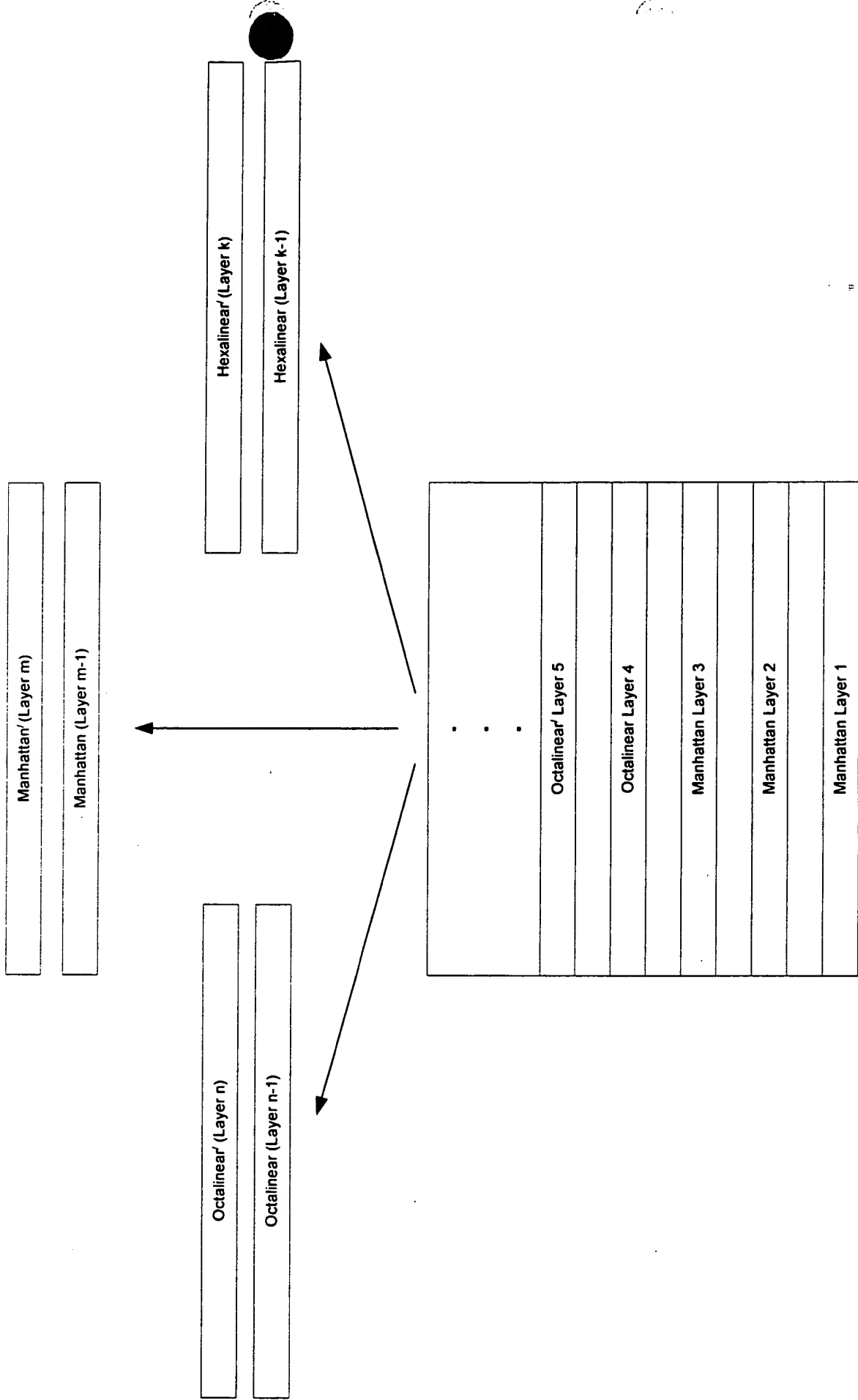
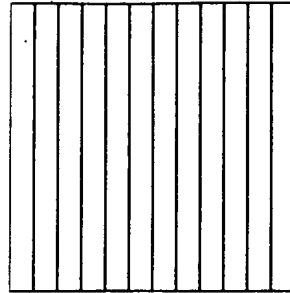
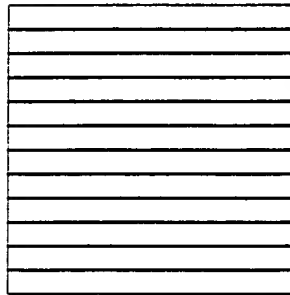


Figure 5b



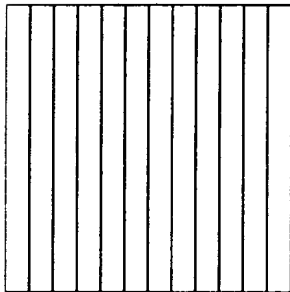
Layer 3

Vertical



Layer 2

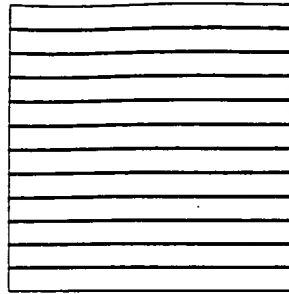
Horizont



Layer 1

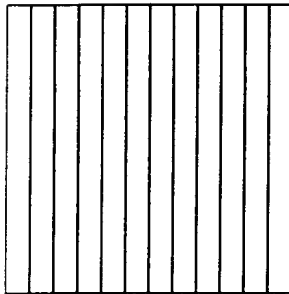
Vertical

Figure 6b



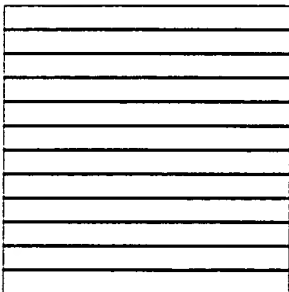
Layer 3

Horizont



Layer 2

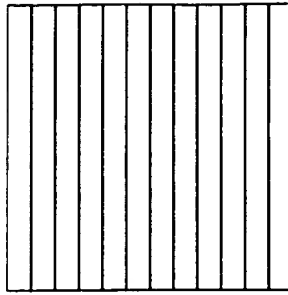
Vertical



Layer 1

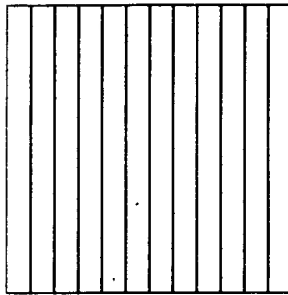
Horizont

Figure 6a



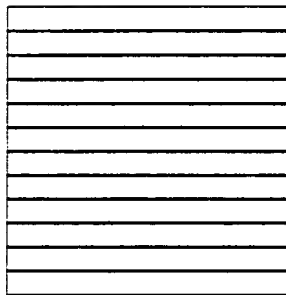
Layer 3

Vertical



Layer 2

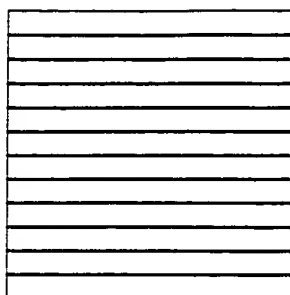
Vertical



Layer 1

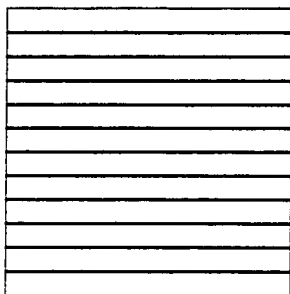
Horizont

Figure 6c



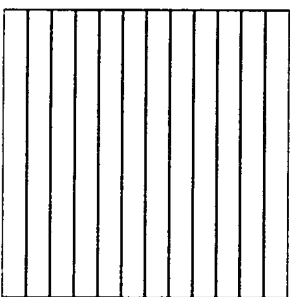
Layer 3

Horizont



Layer 2

Horizont



Layer 1

Vertical

Figure 6d

U.S. Department of the Interior
Bureau of Land Management
Washington, D.C. 20250

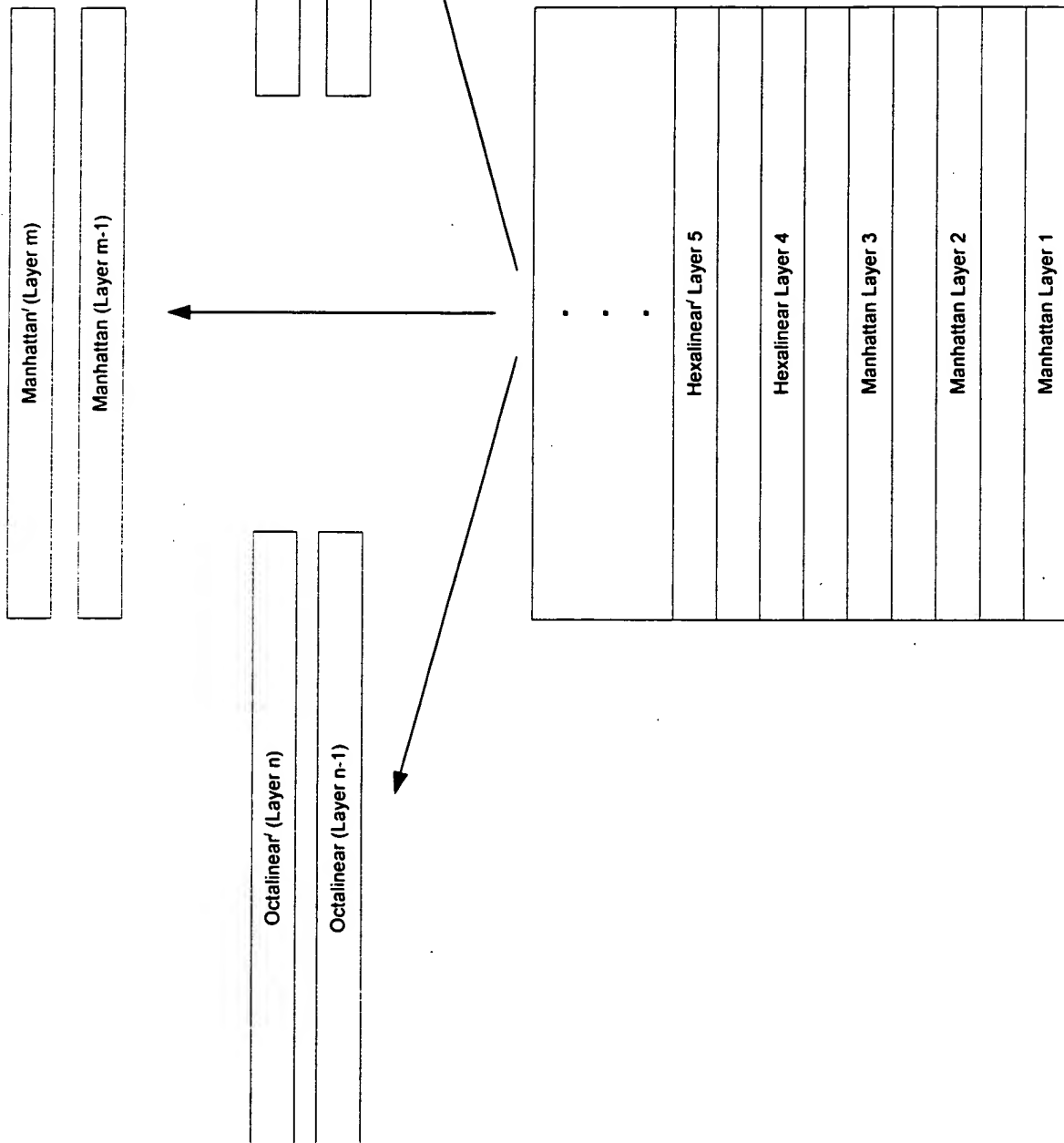


Figure 7

Figure 8: A diagram illustrating the structure of a multi-layered system. The diagram shows a central stack of layers, with arrows pointing from the top and bottom layers to external components.

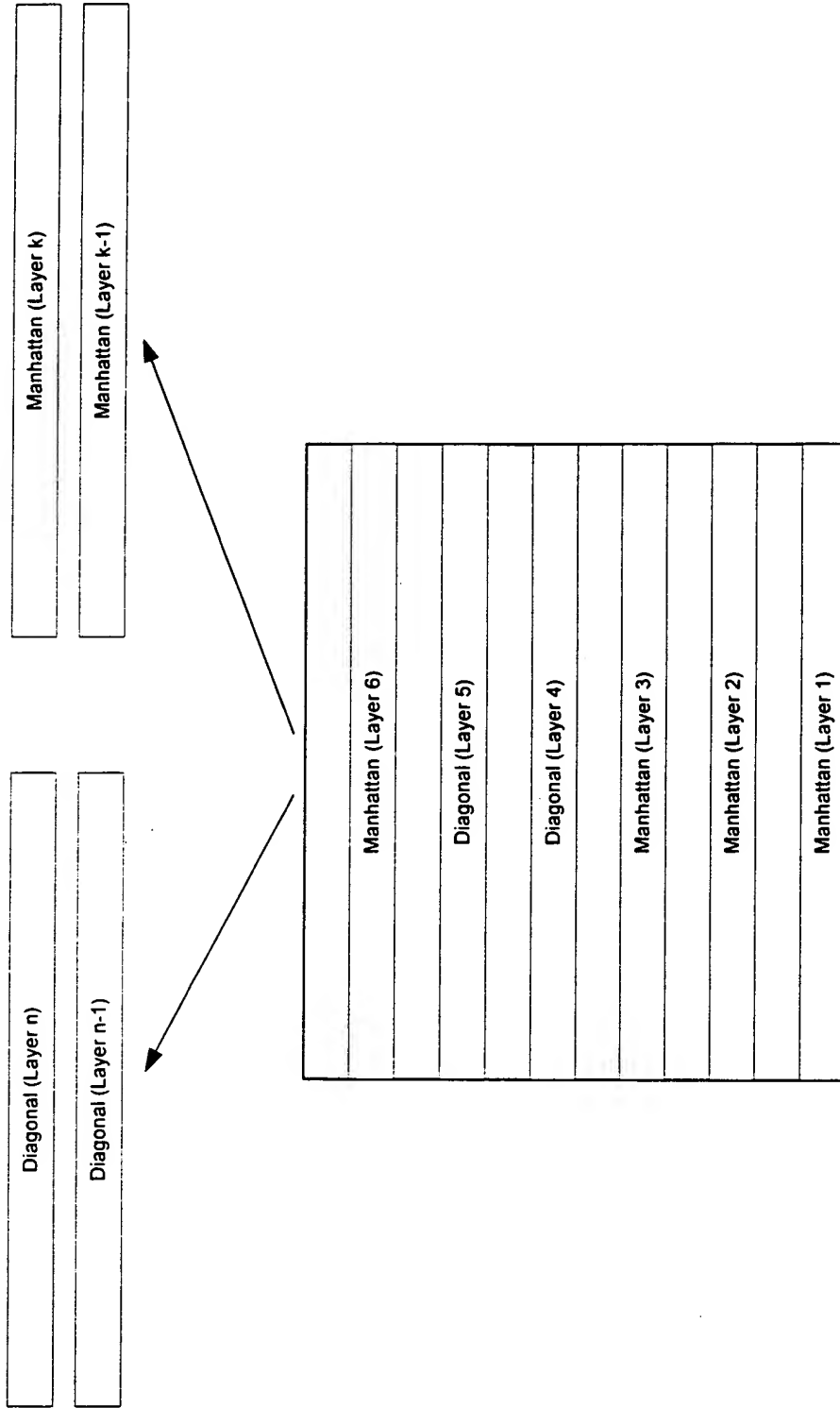


Figure 8

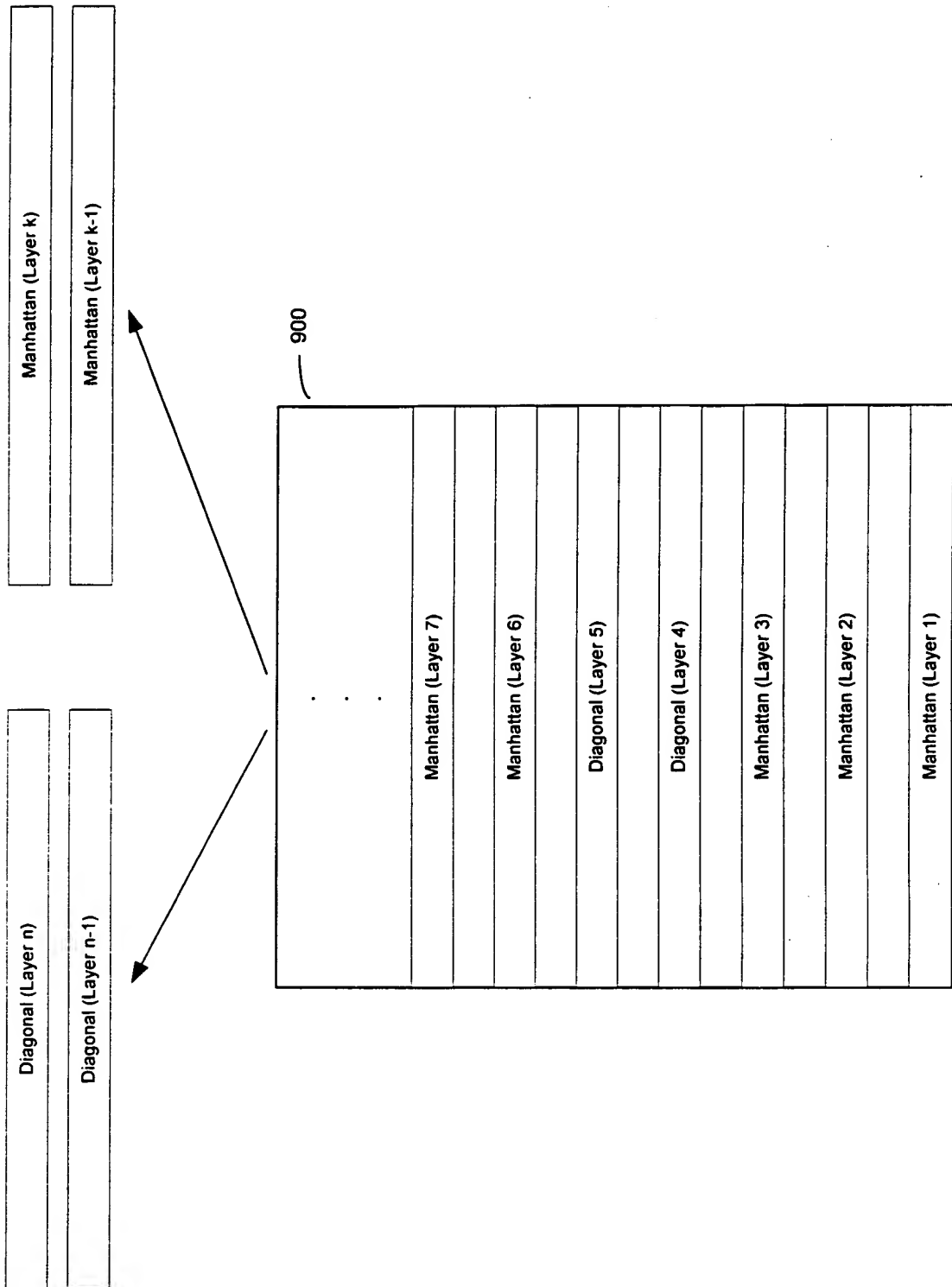


Figure 9

FIG. 10 is a top view of an integrated circuit (IC) 1000, showing a first region 1010, a second region 1020, a third region 1030, and a fourth region 1040. The first region 1010 contains a first set of lines 1012. The second region 1020 contains a second set of lines 1020. The third region 1030 contains a third set of lines 1030. The fourth region 1040 contains a fourth set of lines 1042. The IC 1000 is divided into four regions by a vertical line 1010 and a horizontal line 1020.

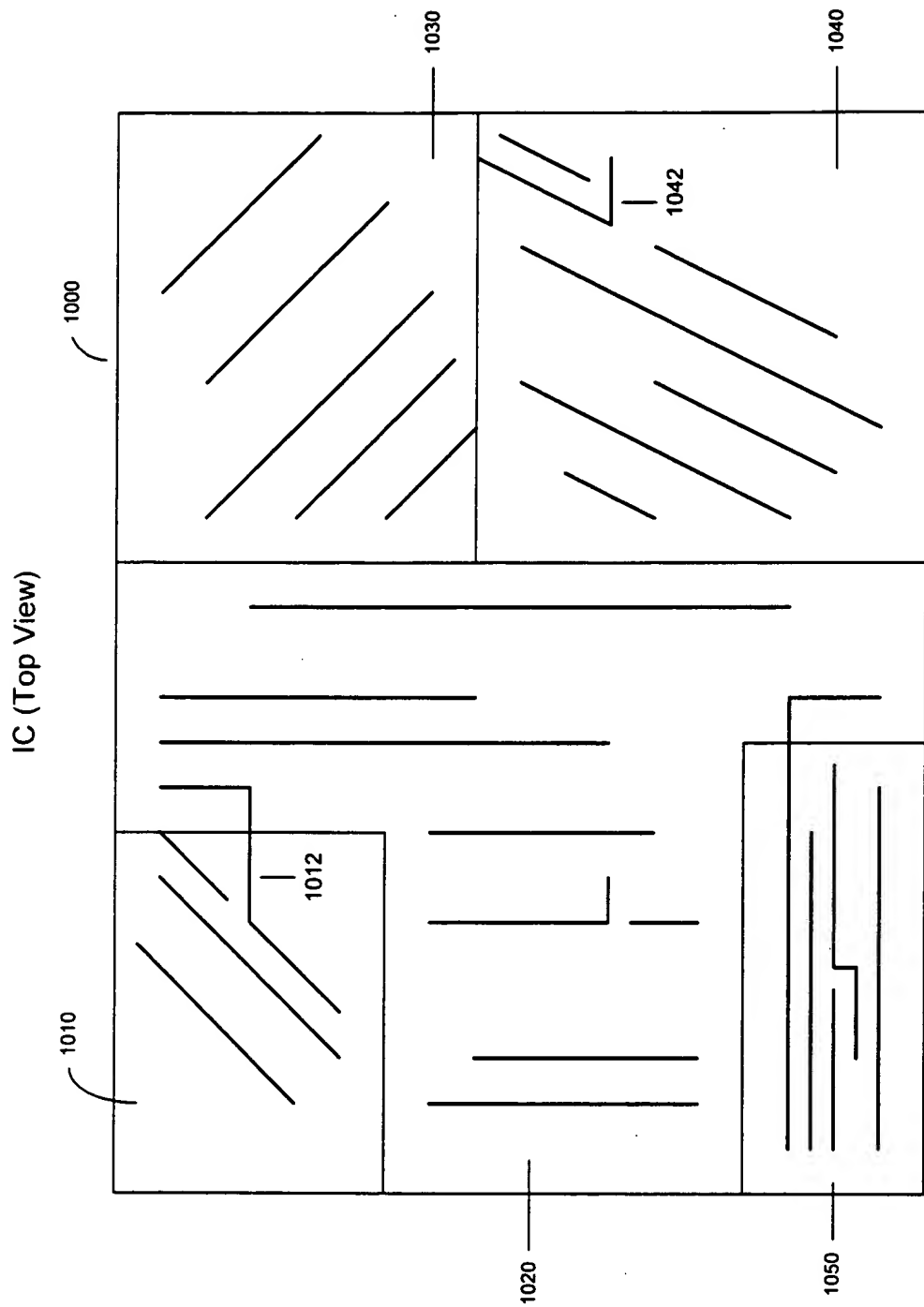


Figure 10

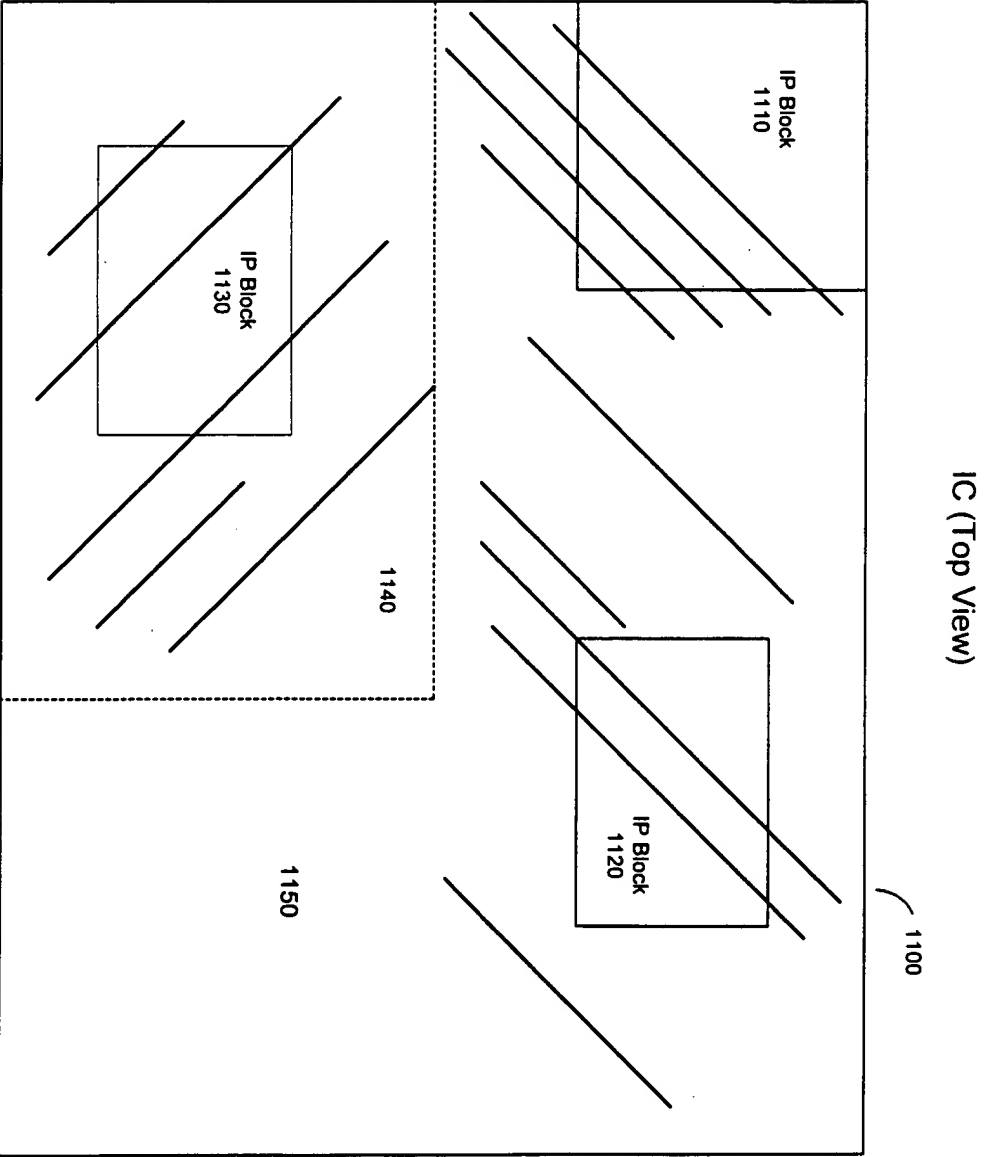


Figure 11

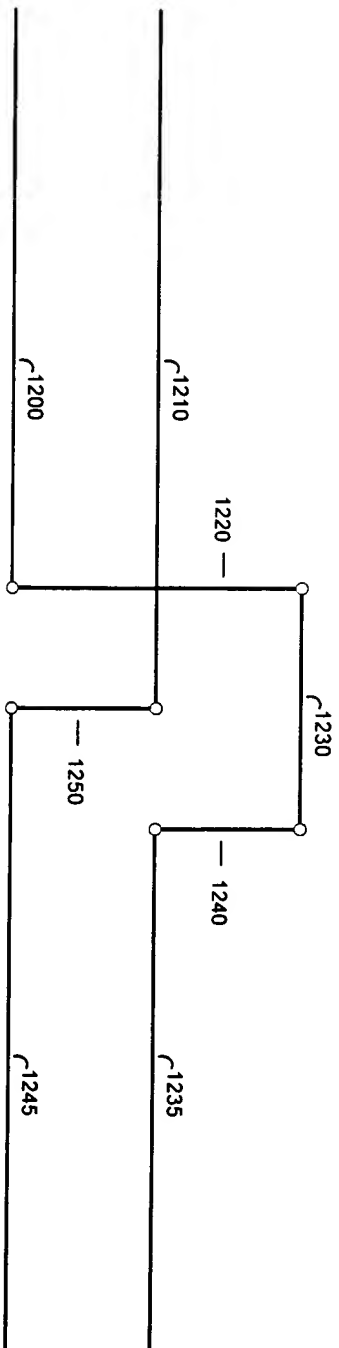


Figure 12a

Prior Art

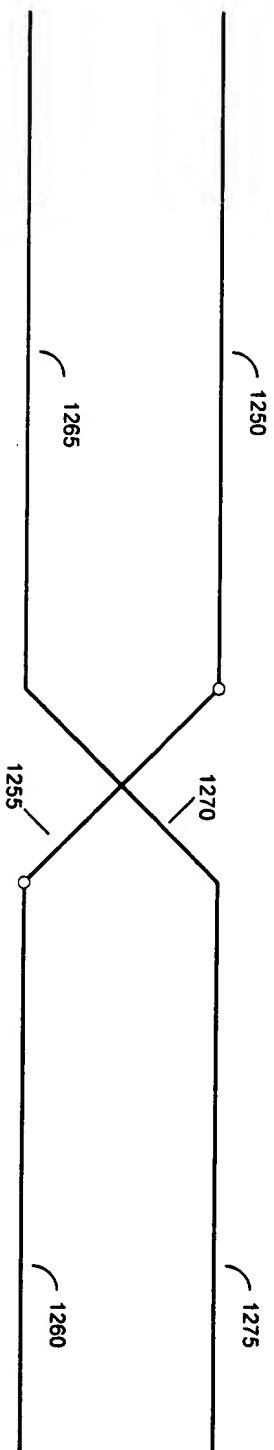
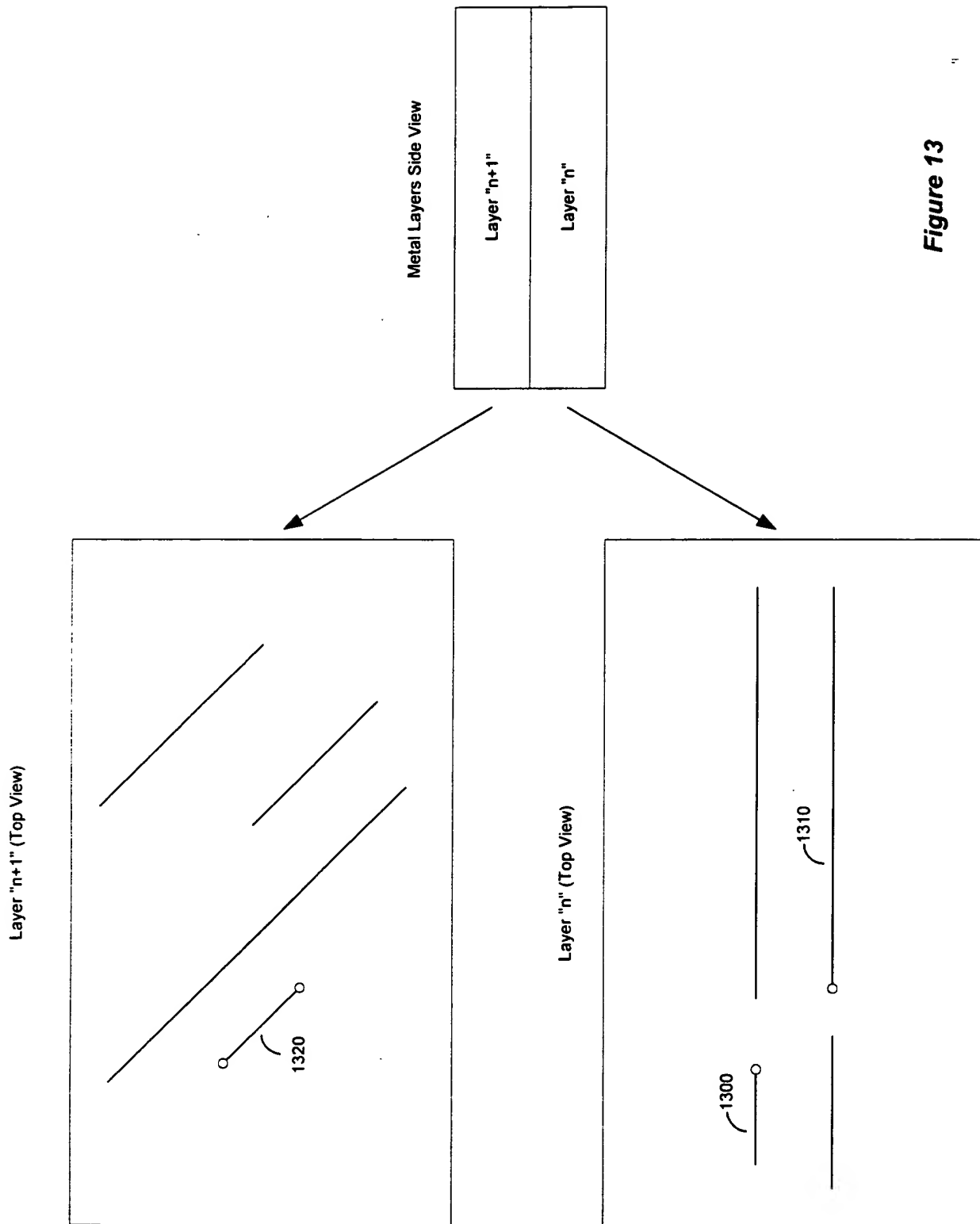


Figure 12b



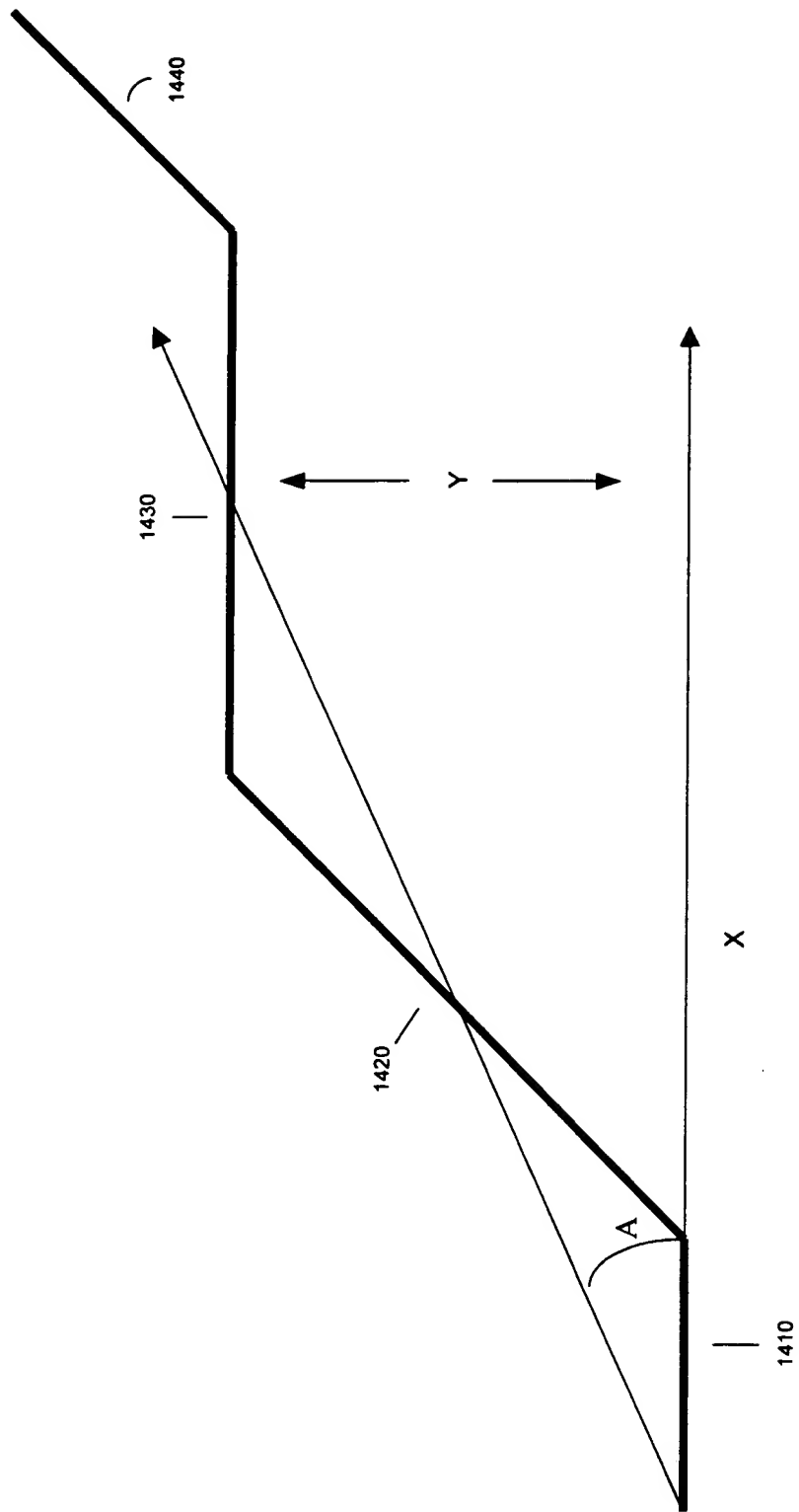


Figure 14

FIG. 15 is a top view of a device 1500, showing a series of parallel, zigzagging lines 1510 and 1520. The lines 1510 are the upper lines of the zigzag pattern, and the lines 1520 are the lower lines. The lines are arranged in a regular, repeating pattern across the device area.

IC (Top View)

1500

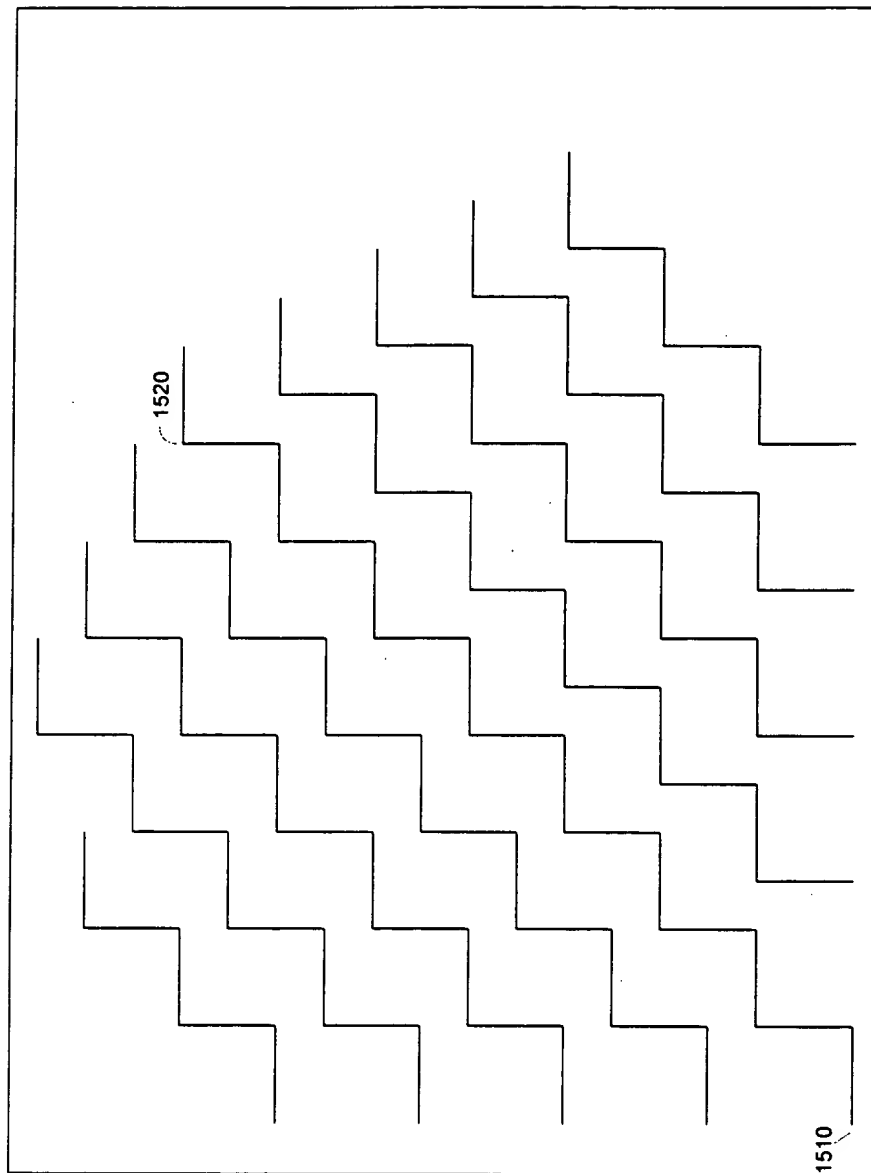


Figure 15

IC (Top View)

1600

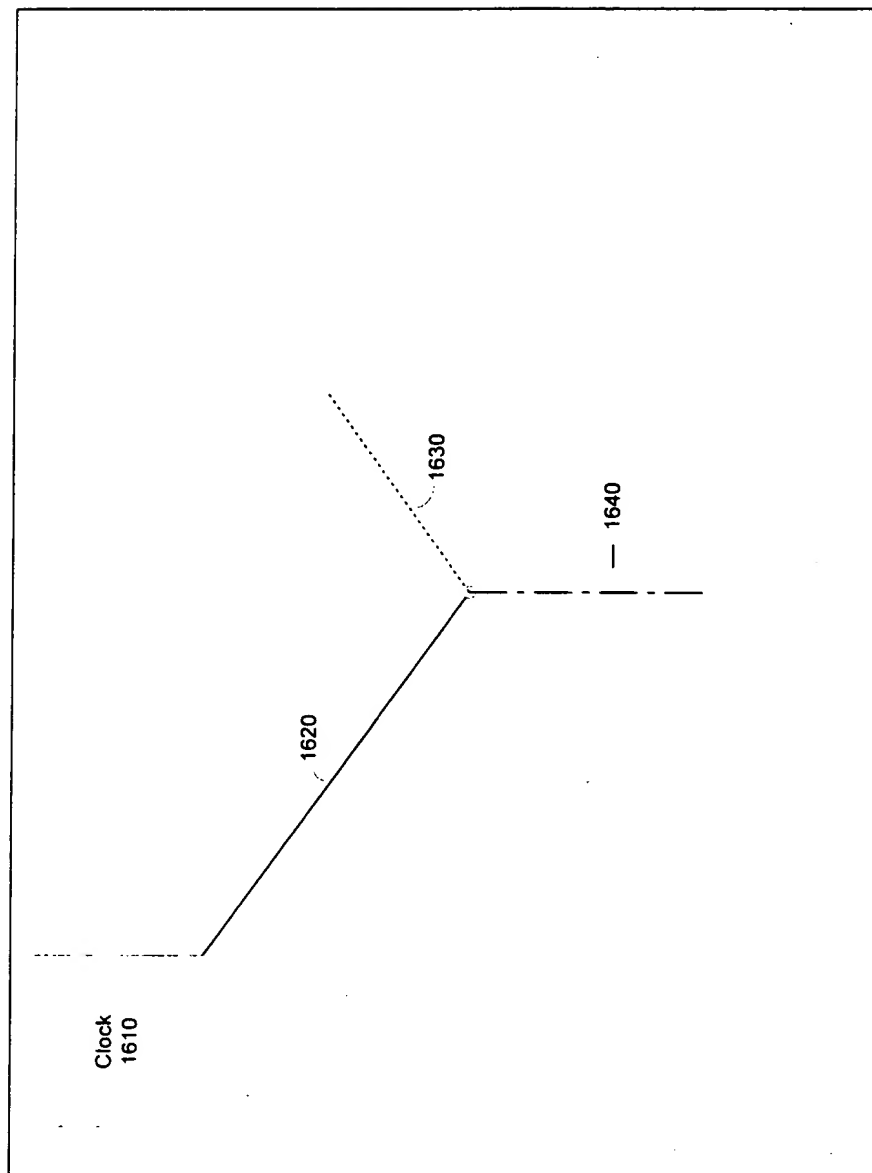


Figure 16